REMARKS

In the Office Action dated October 14, 2008, claims 1-54 and 56-74 were pending and claims 1, 2, 5, 7, 11, 13, 14, 17, 19, 23, 25, 31, 35, 60, 61, 68, 72 and 74 were under consideration.

Applicants have amended 1 and 68. Support for the amendments is found, for example, at Page 29, Paragraph 3 to Page 30, Paragraph 2 of the specification and Figures 6-10 of the drawings. Applicants have further cancelled claims 3-4, 6, 8-10, 12, 15-16, 18, 20-22, 24, 26-30, 32-34, 36-67, and 69-73. No new matter has been introduced by the amendment. Accordingly, favorable reconsideration of all the pending claims is respectfully requested.

Initially, Applicants appreciate the Examiner's indication that claims 13, 14, 17, 19, 23, 25, 31, 35 and 74 are allowable. The Examiner has objected to claims 11 and 68 as being dependent upon a rejected base claim, but indicated that the claims would be allowable if rewritten in independent form including all of the limitations of any intervening claims. In this regard, Applicants have amended claim 68 to incorporate the features recited by claim 61, from which claim 68 depends. Thus, the amendment has placed claim 68 in condition for allowance.

The Examiner has rejected claims 1, 60 and 72 under 35 U.S.C. § 103(a) as allegedly unpatentable over U.S. Patent No. 6,383,916 to Lin (hereinafter "Lin") in view of U.S. Patent Application Publication 2001/0002727 to Shiraishi (hereinafter "Shiraishi").

Applicants respectfully submit that the teachings of Lin and Shiraishi, taken alone or in combination, fail to teach or suggest the invention recited by the instant claims.

Claim 1, as amended, recites a semiconductor unit having two device terminals for every one input/output signal. The semiconductor unit includes a laminated substrate and a semiconductor chip. The substrate includes at least two wiring layers, which include a signal wiring layer and a power-supply or ground wiring layer. The substrate has a main surface. The

semiconductor chip has an input/output pad and is mounted on the main surface of the laminated substrate, with the input/output pad contacting the main surface. The two device terminals are mounted on the laminated substrate and connected to both ends of a signal wire in the signal wiring layer. The substrate further includes a via hole, with one end thereof connected to the signal wire and the other end thereof connected to the input/output pad of the semiconductor chip.

The present invention contemplates a novel semiconductor configuration wherein two terminals for input/output signals are connected to each other through a signal wire in the wiring layer in a laminated substrate and the wire is further connected to the input/output pad through a via hole also formed in the laminated substrate.

The Examiner has acknowledged that Lin fails to disclose, "a signal wire is connected to the input/output pad of said semiconductor chip through a via hole formed in the laminated substrate" (see, Page 3, Lines 2-4 of the Official Action). The Examiner has turned to Shiraishi for the alleged teaching of the above feature. Specifically, the Examiner has relied on Element (109) in Fig. 4 and Paragraph 44 of Shiraishi for the alleged teaching of "a substrate wherein the wiring layers are connected to the chip through a via hole" (see, Page 3, Lines 4-6). Accordingly, the Examiner has alleged that it would be obvious to one of ordinary skill in the art at the time the invention was made to use via holes in the substrate of Lin as taught by Shiraishi in order to achieve the predictable result of reducing wiring length.

Applicants respectfully submit that the teaching of "a substrate wherein the wiring layers are connected to the chip through a via hole" by Shiraishi does not remedy the deficiency of Lin with respect to "a signal wire is connected to the input/output pad of said semiconductor chip through a via hole formed in the laminated substrate".

Shiraishi is directed to a semiconductor device including a multilayered wiring board (107) disposed between semiconductor elements (101, 103) and a semiconductor element (105). The board (107) has a plurality of via holes (109) formed within. As illustrated in Figure 4 and described in Paragraphs 0044 and 0069, Shiraishi discloses that the via hole (109) is connected to a circuit pattern (108), which in turn is connected through a solder junction (110) to an electrode (102) of the semiconductor chip (101). Thus, the via hole (109) in a substrate (107) is not directly connected to an input/output pad of the semiconductor chip. Concomitantly, the input/output pad of the semiconductor chip does not contact a main surface of a laminated substrate.

In contrast, claim 1 recites a via hole formed in the substrate, with one end thereof connected to the signal wire and the other end thereof connected to the input/output pad of the semiconductor, as opposed to the via hole of Shiraishi, with one end thereof connected to a wiring layer and the other end thereof connected to a circuit pattern on the surface of the substrate.

Thus, neither Lin nor Shiraishi, taken alone or in combination, teach or suggest the combination of features recited by claim 1. Accordingly, the rejection of claim 1 under 35 U.S.C. § 103(a) as allegedly unpatentable based on the combination of Lin and Shiraishi is overcome, and withdrawal thereof is respectfully requested.

In addition, Applicants have canceled claims 60 and 72. The cancellation of the claims overcomes any rejection thereof.

The Examiner has further rejected claims 2 and 61 under 35 U.S.C. § 103(a) as allegedly unpatentable over Lin and Shiraishi in view of U.S. Patent No. 6,137,164 to Yew (hereinafter "Yew"). The rejection is respectfully traversed in light of the following remarks.

Claim 1, from which claim 2 depends, is discussed above relative to Lin and Shiraishi.

Yew discloses an assembly for stacking IC devices. Yew is relied on to allegedly teach a substrate having two semiconductor chips mounted on the main surface and back surface, respectively. However, Yew fails to overcome the underlying deficiencies identified in Lin and Shiraishi. Therefore, none of Lin, Shiraishi and Yew, taken alone or in any combination, teach or suggest the combination of features recited by claim 2. Accordingly, the rejection of claim 2 under 35 U.S.C. § 103(a) based on the combination of Lin, Shiraishi and Yew is overcome and withdrawal thereof is respectfully requested.

In addition, Applicants have canceled claim 61. The cancellation of the claim overcomes any rejection thereof.

The Examiner has further rejected claim 5 under 35 U.S.C. § 103(a) as allegedly unpatentable over Lin and Shiraishi in view of U.S. Patent No. 6,630,628 to Devnani (hereinafter "Devnani"). The rejection is respectfully traversed in light of the following remarks.

Claim 1, from which claim 5 depends, is discussed above relative to Lin and Shiraishi.

Devnani discloses a high-performance laminate for integrated circuit interconnection. Devnani fails to overcome the underlying deficiencies identified in Lin and Shiraishi. Therefore, none of Lin, Shiraishi and Devnani, taken alone or in any combination, teach or suggest the combination of features recited by claim 5. Accordingly, the rejection of claim 5 under 35 U.S.C. § 103(a) based on the combination of Lin, Shiraishi and Devnani is overcome and withdrawal thereof is respectfully requested.

The Examiner has further rejected claim 7 under 35 U.S.C. § 103(a) as allegedly unpatentable over Lin and Shiraishi in view of U.S. Patent No. 6,184,477 to Tanahashi (hereinafter "Tanahashi"). The rejection is respectfully traversed in light of the following remarks.

Claim 1, from which claim 7 depends, is discussed above relative to Lin and Shiraishi.

Tanahashi discloses a multi-layer circuit substrate having orthogonal grid ground and power planes. Tanahashi is relied on to allegedly teach or suggest a signal layer between a power layer and a ground layer, the signal layer forming a strip line. Tanahashi fails to overcome the underlying deficiencies identified in Lin and Shiraishi. Therefore, none of Lin, Shiraishi and Tanahashi, taken alone or in combination, teach or suggest the combination of features recited by claim 7. Accordingly, the rejection of claim 7 under 35 U.S.C. § 103(a) based on the combination of Lin, Shiraishi and Tanahashi is overcome and withdrawal thereof is respectfully requested.

In view of the foregoing amendments and remarks, it is respectfully submitted that all claims presently pending in the application are believed to be in condition for allowance, which action is earnestly solicited.

Respectfully submitted,

Paul J. Esatto, Jr.
Registration No. 30,749

SCULLY, SCOTT, MURPHY & PRESSER, P.C.
400 Garden City Plaza, Suite 300
Garden City, New York 11530
516-742-4343
PJE/HC/ech